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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,590	12/04/2003	Tomofusa Shiga	01-522	6921

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EXAMINER	
TRAN, MAI HUONG C	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/726,590	SHIGA ET AL.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/4/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1–7 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-18 of U.S. Patent No. 6,469,345. Although the conflicting claims are not identical, they are not patentably distinct from

each other because the subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows: a semiconductor substrate having a trench formed thereon; and a gate insulating film disposed on an inner wall of the trench, the gate insulating film including a portion being composed of a first oxide film, a nitride film, and a second oxide film which are layered.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 4,785,337 to Kenney.

Regarding to claim 1, Kenney discloses a semiconductor device having a trench gate structure 20, the semiconductor device comprising a laminate film 26 comprised of a first silicon oxide film, silicon nitride film and a second silicon oxide film successively

laminated in this order and formed on a side wall of a trench formed on one surface of a semiconductor substrate 10 (col. 7, lines 48-66, col. 11, lines 35-37); and polysilicon 22/24 that is doped with boron and embedded in the trench through the laminate layer (col. 8, lines 44-47), wherein the silicon nitride film in the laminate layer has a film thickness and film quality sufficient for suppressing boron from passing through the silicon nitride film and wherein the first silicon oxide film (col. 11, lines 41-42 [oxide layer = 4nm]) at the trench side in the laminate film has a film thickness that is greater than a film thickness of the second silicon oxide film (col. 11, lines 49-50 [oxide = 2nm]), at the polysilicon side (figs. 2 and 9A).

Regarding to claim 2, a P-channel MOSFET comprising boron diffusion suppressing film at a gate side of a gate insulating film disposed between a boron-doped polysilicon gate and a channel region (col. 10, lines 15-68, col. 11, lines 1-30, and fig. 9A).

Regarding to claim 3, the P-channel MOSFET, wherein the boron diffusion suppressing film comprises a laminate film that is comprised of a first silicon oxide film, silicon nitride film and a second silicon oxide film successively laminated in this order (col. 11, lines 30-50).

Regarding to claim 4, the P-channel MOSFET, wherein a film thickness of the first silicon oxide film at a gate side is thinner then a film thickness of the second silicon oxide film at a channel side (col. 11, lines 41-50).

Regarding to claim 5, the P-channel MOSFET, wherein the boron-doped polysilicon gate is a trench gate (col. 10, lines 15-68, col. 11, lines 1-30, and fig. 9A).

Regarding to claim 6, Kenney discloses a method of manufacturing a semiconductor device having a trench gate structure 20, wherein the semiconductor device comprises a laminate film 26 comprised of a first silicon oxide film, silicon nitride film and a second silicon oxide film laminated in this order and formed on a side wall of a trench formed on one surface of a semiconductor substrate (col. 7, lines 48-66, col. 11, lines 35-37), and polysilicon 22/24 that is doped with boron and embedded in the trench through the laminate layer (col. 8, lines 44-47), the method comprising: forming the trench on one surface of the semiconductor substrate; forming the first silicon oxide film on the side wall of the trench so that a film thickness of the first silicon oxide film is larger than that of the second silicon oxide film at the polysilicon side; forming the silicon nitride film on the first silicon oxide film so that the silicon nitride film has a film thickness and film quality under the condition of which boron can be suppressed from passing through the silicon nitride film; and forming the second silicon oxide film on the silicon nitride film so that the second silicon oxide film is

smaller in thickness than the first silicon oxide film at the trench side, thereby forming the laminate film (col. 11, lines 41-50, and figs. 2 and 9A).

Regarding to claim 7, the silicon nitride film is formed by CVD (col. 7, lines 48-54).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mai-Huong Tran whose telephone number is (571)272-1796. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mai-Huong Tran

Examiner
Art Unit 2818